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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/050,774	01/18/2002	Shaun Dennie	06502.0207.01	9924

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EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 02/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,774	DENNIE, SHAUN	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-26 and 30-34* is/are pending in the application.

4a) Of the above claim(s) *17-22 and 27-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23,25,26,30 and 32-34* is/are rejected.

7)☐ Claim(s) *24 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/15/3 and 10/29/4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Response to Amendment

1. This office action is in response to Applicant's communication filed November 10, 2005. This amendment has been entered and carefully considered. Claims 23-26 and 30-34 remain pending in the application.

2. The IDS (January 15, 2003 and October 29, 2004) submitted with stamped postcard have been received and considered.

3. Applicant's arguments with respect to claims 23-26 and 30-34 have been considered but are deemed to be moot in view of the new grounds of rejection. The finality of the previous office action is hereby withdrawn. Any inconvenience is *SINCERELY* regretted.

Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the

invention was made.

5. Claims 23 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Snider (USPN: 5,991,893); hereinafter in view of Walls (USPN: 5,675,790).

As per claim 23, Snider discloses a system 100 for assigning blocks of memory, the system 100 comprising an area of a memory (allocation table of the VRSM layer 101, figure 1, column 8, lines 2-3) designated for coordinating the assignment of the memory to one or more threads 104 requiring access to the memory 106 (e.g. see figure 1, column 4, lines 65 bridging column 5, line 1) wherein the VRSM layer 101 including usage information reflecting usage of the memory; for example, VRSM 101 to allocate a data structure of the specified size from the heap of virtually reliable memory including additional parameters supplying information (e.g. memory size, usage etc ...) about the requested data structure (e.g. see column 5, lines 33-40); Snider further discloses locking protocol as being equivalent to the processor as claimed for controlling access to the memory (e.g. see column 6, lines 65-67; column 7, lines 7-9). Snider discloses the invention as claimed except for the serialized operation by the processor/controller to allow a first thread to access a first designated block of the memory while another thread requests and secures access to another block of the memory. Walls, in his teaching of method for improving the performance of dynamic

memory allocation, clearly discloses the concept of serializing accesses to the dynamic memory section (e.g. see column 2, lines 42-44); allowing a first thread to access the first section of the dynamic memory while another process secure access to another section of dynamic as being equivalent to when two users make simultaneous requests for dynamic memory, preventing the allocation to the same section of dynamic memory to two or more processes wherein it's understood that each process must be allocated for access to different section of dynamic memory (e.g. see column 2, line 67 bridging column 3, line 4). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to utilize the teaching as taught by Walls as being detailed above for that of Snyder's system in order to arrive at Applicant's current invention. In doing would allow multiple operations be processed without having to wait for the completion of one operation in order to process the next operation which results to enhancing system throughput, therefore being advantageous.

As per claim 25, the combination of Snider and Walls disclose the size the designated block of memory and another designated block are determined by the virtually reliable shared memory (VRSM) software layer 101 (e.g. see column 5, lines 32 et seq.; column 6, lines 57 et seq.); Walls discloses the allocation blocks with the block size 24, 25, 26, 27, 28, 29 (figure 2, and

similarly for 34S, 36S, 38S... are selected and allocated by the consumers (e.g. see figures 2 and 3, column 5, lines 55 et seq.). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement and allow such functions of determining the size for the allocated block to be controlled and manually programmed by the user instead software control so it would allow the system of Snider to serve broader range of applications, specially system test and analysis which results to enhancing overall system reliability, therefore being advantageous.

As per claim 26, Walls discloses wherein the another designated block of memory is adjacent to the designated block of memory (e.g. see column 7, lines 2 et seq.);

6. Claims 30 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Resman (USPN: 5,535,64), hereinafter Resman, in view of Walls (USPN: 5,675,790);

As per claim 30; Resman discloses the invention as claimed including a method comprises allocating to a first process a first block of a memory that has a size designated by a user is taught as allocating a higher priority procedures first portion of RAM by an I/0 device or host device (without accessing an operating system) with a size designated by a user if RAM size available from the first portion (e.g. see abstract, column 2,

lines 37-40; column 3, lines 6-8); allocating to second process a second block of the memory that has a size designated by the user is equivalently taught as allocating a lower priority procedures to a second portion of RAM by an I/0 device or host device (without accessing an operating system) with a size designated by a user when available RAM size in the first portion exceeds a first threshold level (e.g. see abstract, column 2, lines 41-44, column 3, lines 6-8). Resman discloses the invention as claimed except for the serialized operation by allowing a first thread to access a first designated block of the memory while another thread requests and secures access to another block of the memory. Walls, in his teaching of method for improving the performance of dynamic memory allocation, clearly discloses the concept of serializing accesses to the dynamic memory section (e.g. see column 2, lines 42-44); allowing a first thread to access the first section of the dynamic memory while another process secure access to another section of dynamic as being equivalent to when two users make simultaneous requests for dynamic memory, preventing the allocation to the same section of dynamic memory to two or more processes wherein it's understood that each process must be allocated for access to different section of dynamic memory (e.g. see column 2, line 67 bridging column 3, line 4). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current

invention was made to utilize the teaching as taught by Walls as being detailed above for that of Snyder's system in order to arrive at Applicant's current invention. In doing would allow multiple operations be processed without having to wait for the completion of one operation in order to process the next operation which results to enhancing system throughput, therefore being advantageous.

As per claim 32, Resman clearly discloses the first and second blocks of memory (free RRM pool and 26) are consecutive block of memory (e.g. see figure 1);

As per claim 33, the further limitation of incrementing A VALUE, being equated the available RAM, wherein in allocating a first portion to a higher priority process by determining if available RRM is available from the first portion (e.g. see column lines 39-41);

As per claim 34, the further limitation of determining the second block of memory based on the incremented value (incremented of available RRM in the first portion) is taught by Resman; for example, Resman clearly discloses enabling allocation of RRM from the second portion to a lower priority procedure when available RAM In the first portion exceeds a first threshold level (e.g. see column 2, lines 40-43);

Allowable subject matter

7. Claims 24 and 31 are objected to as being dependent upon a rejected base claims 23 and 30, but would be allowable if rewritten in independent form including all of the limitations of the base claim and intervening claims. The prior arts of record do not teach nor clearly disclose the allocating of the first and second blocks of memory to the first and second processes is based on a token obtained from a designated area of the memory.

8. With respect to the remark, Examiner again would like to emphasize that the allocation table of the VRSM layer 101 can well be consider as a memory designated for coordinating the assignment of the memory to one or more threads; for example, the allocation table which is part of the VRSM layer 101 is a memory location accessed by multiple threads wherein the VRSM layer 101 to allocate a data structure of the specified size from the heap of virtually reliable memory; wherein memory is allocated from the shared memory pool, it is transparent to the operating system, and the VRSM layer can assemble data structure from shared memory within only one node or from multiple portions of shared memory from multiple nodes (e.g. see column 5, lines 33-52). The further arguments of "Snider does not show the processors 105 executing threads that access VRSM 101" et seq. (remark, page 5, 2nd and 3th paragraph; 10/11/2005)) is moot in view of the new prior art of Walls ('790). With respect to the

"usage information" (page 6, lines 3 et seq.), Examiner again would like to point out that Snider discloses the VRSM 101 to allocate a data structure of the specified size from the heap of virtually reliable memory *including additional parameters supplying information (e.g. memory size, usage etc ...)* about the requested data structure (e.g. see column 5, lines 33-40). With respect to arguments the size of the designated memory being determined by the user, Walls discloses the allocation blocks with the block size 24, 25, 26, 27, 28, 29 (figure 2, and similarly for 34S, 36S, 38S... are selected and allocated by the consumers (e.g. see figures 2 and 3, column 5, lines 55 et seq.). With respect to the arguments regarding claims 30-34, it has been moot in view of the newly applied prior art of Walls ('790); in addition, the allocating of a first block of memory having a size designated by a user without accessing an operating system is taught by Resman as allocating a higher priority procedures to a first portion of RAM by an I/O device or host device transparent of the operating system with a size designated by the user if RAM size available from the first portion (e.g. again, see abstract, column 2, lines 37-40 and column 3, lines 6-8), Resman discloses different size portions (RAM size or memory block size as being claimed) are allocated between procedures having higher and lower priorities without interference of the operating system (e.g. see column 2, lines 30-36).

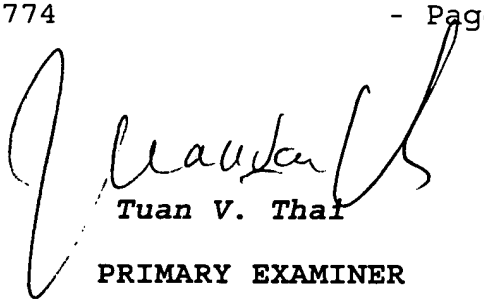
Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (572)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/February 17, 2006



Tuan V. Thai

PRIMARY EXAMINER

Group 2100